UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,575	08/22/2003	R. Jacob Baker	M4065.0962/P962	8212

45374 7590 12/07/2007

DICKSTEIN SHAPIRO LLP
1825 EYE STREET, NW
WASHINGTON, DC 20006

EXAMINER	
PRABHAKHER, PRITHAM DAVID	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
12/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,575	BAKER, R. JACOB	
	Examiner	Art Unit	
	Pritham Prabhakher	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,9,10,12,16-18,21,23,24,42-45 and 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,10,12,16,21,23,24 and 42-44* is/are rejected.

7)☒ Claim(s) *2-5,7,9,17,18,45 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/25/2003 and 08/05/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 12 recites the limitation "the third circuit" in the imager device of claim 10. There is insufficient antecedent basis for this limitation in the claim since there is no third circuit disclosed in claim 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 16 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Washkurak et al. (US Patent No.: 6704050B1).

*In regard to **Claim 1**, Washkurak et al. disclose an image device (Figure 2), comprising:*

*an array of pixels (Figure 2 and **Column 3, Lines 51-53**); and*

*a first circuit electrically coupled to at least one pixel of said array (Column Processing circuit 105, **Figure 3**), said first circuit being adapted to output a representation of an analog pixel signal based on a difference between a reference*

signal current (reference current stored in current mirror 32) and pixel signal current (current signal stored in signal current mirror 130) (The reference signal current and pixel signal current are sent to the differential output amplifier 160 which outputs a signal based on the differences between the two currents, ***Figure 3 and Column 4, Lines 18-60)****.*

Although the reference discloses outputting a signal based on the differences between the two currents, the Washkurak et al. reference is silent in teaching that an A/D converter is present that converts the analog signal to a digital signal. Official notice is taken by the examiner in stating that it would have been obvious and well known at the time of the invention to incorporate an A/D converter into the teachings of Washkurak et al. to obtain a digital output of the signal, because a digital signal reduces the noise and is easier to calibrate and adjust.

With regard to ***Claim 16****, Washkurak et al. disclose an imager device comprising:*

an array of pixels (Figure 2 and ***Column 3, Lines 51-53)****;*

a first circuit coupled to a pixel of said array (Column Processing circuit 105, ***Figure 3)****, said first circuit converting an analog reference signal voltage into a reference current (Reference voltage is converted to reference current by 150,* ***Column 4, Lines 18-60)****;*

a circuit coupled to the pixel, said circuit converting an analog pixel signal voltage into a pixel current (Pixel voltage is converted to pixel current by 150, ***Column 4, Lines 18-60)****.*

However, Washkurak et al. do not disclose that the converting of the pixel voltage to the pixel current is performed by a separate, second circuit. Official notice is taken saying it would have been obvious to one of ordinary skill in the art at the time of the invention to perform the feature of converting the pixel voltage to a Pixel current on a separate circuit that was different from the circuit that converted the reference voltage to the reference current, because it would have increased the speed of processing and decreased the wait time of the processing of the signal.

Although the reference discloses outputting a signal based on the differences between the two currents (The reference signal current and pixel signal current are sent to the differential output amplifier 160 which outputs a signal based on the differences between the two currents, ***Figure 3 and Column 4, Lines 18-60)****, the Washkurak et al. reference is silent in teaching that an A/D converter is present that converts the analog signal to a digital signal. Official notice is taken by the examiner in stating that it would have been obvious and well known at the time of the invention to incorporate an A/D converter into the teachings of Washkurak et al. to obtain a digital output of the signal, because a digital signal reduces the noise and is easier to calibrate and adjust.*

Regarding ***Claim 42****, Washkurak et al. disclose a method of operating an imager, said method comprising the steps of:*

converting a reference signal voltage into a first current (Reference voltage is converted to reference current by 150, ***Column 4, Lines 18-60)****;*

converting a pixel signal voltage into a second current (Pixel voltage is converted to pixel current by 150, ***Column 4, Lines 18-60)****; and*

outputting a representative of the pixel signal based on a difference of the first and second currents (The reference signal current and pixel signal current are sent to the differential output amplifier 160 which outputs a signal based on the differences between the two currents, ***Figure 3 and Column 4, Lines 18-60)****.*

Although the reference discloses outputting a signal based on the differences between the two currents, the Washkurak et al. reference is silent in teaching that an A/D converter is present that converts the analog signal to a digital signal. Official notice is taken by the examiner in stating that it would have been obvious and well known at the time of the invention to incorporate an A/D converter into the teachings of Washkurak et al. to obtain a digital output of the signal, because a digital signal reduces the noise and is easier to calibrate and adjust.

Claims 10, 12, 21,23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Washkurak et al. (US Patent No.: 6704050B1) as applied to claims 1, 16 above, and further in view of Clark et al. (US Patent No.: 6515701B2).

With regard to ***Claim 10****, Washkurak et al. do not disclose the imager device of claim 1 further comprising a counter for counting said digital representation to obtain a multi-bit digital code representative of the analog pixel signal. Clark et al. disclose a CMOS imager device that has a counter for counting a digital representation to obtain multi-bit digital code representative of the analog pixel signal,* ***Figure 2 and Column 5, Lines 37-60 of Clark et al.****. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a counter into the invention disclosed by Washkurak et al., because it enables an output of a region of interest to be generated at a specific time that is preferable to the user.*

Regarding ***Claim 12****, Washkurak et al. and Clark et al. disclose the image device of claim 10 further comprising:*

a hold register for holding the multi-bit digital code while said first circuit outputs a second digital representation of another analog pixel signal (Register discussed in ***Column 5, Lines 45-50 of Clark et al.)****;*

a decoder connected to said hold register for outputting the multi-bit digital code (Decoders are connected to the registers, ***Figure 2 and Column 5, Lines 45 to Column 6, Line 2 of Clark et al.)****; and*

a current mirror for mirroring the reference signal current to the third circuit (Current mirror 132 mirrors the reference signal current to a third circuit, ***Figure 3 and Column 4, Lines 19-60 of Washkurak et al.)****.*

With regard to ***Claim 21****, Washkurak et al. do not disclose the imager device of claim 16 further comprising a counter for counting said digital value to obtain a multi-bit digital code representative of the analog pixel signal. Clark et al. disclose a CMOS imager device that has a counter for counting a digital representation to obtain multi-bit digital code representative of the analog pixel signal,* ***Figure 2 and Column 5, Lines 37-60 of Clark et al.****. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a counter into the invention disclosed by Washkurak et al., because it enables an output of a region of interest to be generated at a specific time that is preferable to the user.*

Regarding ***Claim 23****, Washkurak et al. and Clark et al. disclose the imager device of claim 21 further comprising a hold register for holding the multi-bit digital code while said analog-to-digital converter outputs a second digital value for another analog pixel signal (Register discussed in* ***Column 5, Lines 45-50 of Clark et al.)****.*

In regard to ***Claim 24****, Washkurak et al. and Clark et al. disclose the imager device of claim 23 further comprising a decoder connected to said hold register for outputting the multi-bit digital code (Decoders are connected to the registers,* ***Figure 2 and Column 5, Lines 45 to Column 6, Line 2 of Clark et al.)****.*

Claims 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Washkurak et al. (US Patent No.: 6704050B1) as applied to claim 42 above, and further in view of Fuse (US Patent No.: 5229761)

*In regard to **Claim 43**, Washkurak et al. disclose the method of claim 42, wherein said step of converting the reference signal voltage comprises:*

*inputting the reference signal voltage (The reference voltage is input and converted by 150 into a reference current, **Column 4, Lines 10 to 60)**.*

*However, Washkurak et al. do not teach of applying the reference signal voltage across a switchable resistance resistor. Fuse teaches of alternating a reference voltage using variable resistance resistor to obtain different voltage values as needed, **Column 2, Lines 1-9 of Fuse**. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a means of changing the resistance to alter a voltage, because this would give the user the control of selecting the desired voltage for a particular design choice.*

*In regard to **Claim 43**, Washkurak et al. disclose the method of claim 42, wherein said step of converting the pixel signal voltage comprises:*

*inputting the pixel signal voltage (The pixel voltage is input and converted by 150 into a reference current, **Column 4, Lines 10 to 60)**.*

However, Washkurak et al. do not teach of applying the pixel signal voltage across a switchable resistance resistor. Fuse teaches of alternating a voltage using a variable resistance resistor to obtain different voltage values as needed, ***Column 2, Lines 1-9 of Fuse****. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a means of changing the resistance to alter a voltage, because this would give the user the control of selecting the desired voltage for a particular design choice.*

Allowable Subject Matter

Claims 2-5, 7, 9, 17, 18, 45 and 47 are objected to as being dependent upon a rejected base claims 1, 16 and 42, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pritham Prabhakher whose telephone number is 571-270-1128. The examiner can normally be reached on M-F (7:30-5:00) Alt Friday's Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pritham David Prabhakher
Patent Examiner
Pritham.Prabhakher@uspto.gov

Pritham . D. Prabhakher

DAVID OMETZ
SUPERVISORY PATENT EXAMINER